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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,296	03/09/2004	Dana Lee	2102397-992471	4439
7590	09/19/2006			EXAMINER ROSE, KIESHA L
Ronald L. Yin GRAY CARY WARE FREIDENRICH LLP 2000 University Avenue East Palo Alto, CA 94303-2248			ART UNIT 2822	PAPER NUMBER

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/797,296	LEE ET AL.	
	Examiner Kiesha L. Rose	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 6/7/06.

2a) This action is **FINAL**.      2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1-20 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____.
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.	5) <input type="checkbox"/> Notice of Informal Patent Application
	6) <input type="checkbox"/> Other: _____.

## DETAILED ACTION

This Office Action is in response to the request for reconsideration filed 7 June 2006.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Hu et al. (U.S. Patent 6,952,034)

The applied reference has a common assignee with the instant application.

Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In re claim 1, Hu discloses a memory array (Fig. 2q) that contains a substantially single crystalline semiconductive material (10) of a first conductivity type (P), having a substantially planar surface with a trench in said surface of said material; said trench having a sidewall and a bottom wall; a first region (70) of a second conductivity type (N), different from said first conductivity type in said material along said planar surface; a second region (52) of said second conductivity type (N) in said material along said bottom wall of said trench; a channel region, having a first portion (94) and a second portion (92), connecting said first and second regions for the conduction of charges, wherein said first portion is along said surface adjacent to said first region, and said second portion is along said sidewall adjacent to said second region; a dielectric (30) on said channel region; a floating gate (40) in said trench, on said dielectric, spaced apart from said second portion of said channel region; a first gate electrode (68) on said dielectric, spaced apart from said first portion of said channel region; and a second gate electrode (54), in said trench, capacitively coupled to said floating gate.

In re claim 2, the single crystalline semiconductive material is silicon.

In re claim 3, the floating gate having a tip (area 96) substantially adjacent to first gate electrode. (Fig. 2)

In re claim 4, a second dielectric (46/56) between tip and first gate electrode permitting the Fowler-Nordheim tunneling of electrons from floating gate to first gate electrode. (Column 9, lines 41-49)

In re claim 5, a second dielectric (36) between floating gate and bottom wall of trench permitting the Fowler-Nordheim tunnel of electrons from floating gate and second region.

In re claim 6, Hu discloses a memory array (Fig. 2q) that contains an array of non-volatile memory cells (Fig. 4), arranged in a plurality of rows and columns, said array comprising: a substantially single crystalline semiconductive material (10) of a first conductivity type (P), having a substantially planar surface with a plurality of trenches in said surface of said material; each of said trenches having a sidewall and a bottom wall; a plurality of non-volatile memory cells arranged in a plurality of rows and columns in said semiconductive substrate material with each cell comprising: a first region (70) of a second conductivity type (N), different from said first conductivity type in said material along said surface; a second region (52) of said second conductivity type (N) in said material along said bottom wall of said trench; a channel region, having a first portion (94) and a second portion (92), connecting said first and second regions for the conduction of charges, wherein said first portion is along said surface adjacent to said first region, and said second portion is along said sidewall adjacent to said second region; a dielectric (30) on said channel region; a floating gate (40) on said dielectric, spaced apart from said second portion of said channel region; a first gate electrode (68) on said dielectric, spaced apart from said first portion of said channel region; and a second gate electrode (54), in said trench, capacitively coupled to said floating gate. wherein said cells in the same row have said first gate electrode in common; wherein said cells in the same column have said first region in common, said second region in

common, said second gate electrode in common; and wherein said cell in adjacent columns have said first region in common to one side; and said second gate electrode and said second region in common to another side. (Fig. 4)

In re claim 7, the single crystalline semiconductive material is silicon.

In re claim 8, the floating gate having a tip (area 96) substantially adjacent to first gate electrode. (Fig. 2)

In re claim 9, a second dielectric (46/56) between tip and first gate electrode permitting the Fowler-Nordheim tunneling of electrons from floating gate to first gate electrode. (Column 9, lines 41-49)

In re claim 10, a second dielectric (36) between floating gate and bottom wall of trench permitting the Fowler-Nordheim tunnel of electrons from floating gate and second region.

In re claim 11, an isolation region (26, Fig. 4) separates adjacent rows of cells.

In re claim 12, Hu discloses a memory cell (Fig. 2) that contains an array of non-volatile memory cells (Fig. 4) in a substantially single crystalline semiconductive substrate material (10) of a first conductivity type (P), wherein said array of non-volatile memory cells has a plurality of non-volatile memory cells arranged in a plurality of rows and columns in said semiconductive substrate material, said method comprising: forming spaced apart isolation regions (26) on said semiconductive substrate that are substantially parallel to one another and extend in said column direction, with an active region (22/24) between each pair of adjacent isolation regions, wherein said semiconductive substrate has a substantially planar surface; forming a plurality of

memory cells in each of the active regions, wherein the formation of each of the memory cells includes: forming a trench into the surface of the substrate, said trench having a sidewall and a bottom wall; forming a floating gate (40) in the trench along the sidewall and insulated therefrom; forming a first region (52) in said substrate along the bottom wall of the trench, with said first region being of a second conductivity type (N), different from said first conductivity type; forming a first gate electrode (54) in the trench, said first gate electrode insulated from said first region and capacitively coupled to said floating gate; forming a second region (70), of the second conductivity type (N) in said substrate, along the surface thereof, spaced apart from the trench; and forming a second gate electrode (68) spaced apart from the surface between said second region and said trench.

In re claim 13, a step of forming first gate electrode includes forming first gate electrode continuously in row direction across a plurality of columns. (Fig. 4)

In re claim 14, a step of forming second gate electrode includes forming second gate electrode continuously in column direction across a plurality of rows. (Fig. 4)

In re claim 15, a step of forming said first region and said second region includes forming said first region and said second region continuously in said row direction across a plurality of columns. (Fig. 4)

In re claim 16, the cells in the same row have said second gate electrode in common; and wherein said cells in the same column have said first region in common, said second region in common, said first gate electrode in common; and wherein said

cell in adjacent columns have said second region in common to one side; and said first gate electrode and said first region in common to another side. (Fig. 4)

In re claim 17, Hu discloses a memory cell (Fig. 2) that contains a non-volatile memory cell (Fig. 4) in a substantially single crystalline semiconductive substrate (10) of a first conductivity type (P), said substrate having a substantially planar surface, said method comprising: forming a trench into the surface of the substrate, said trench having a sidewall and a bottom wall; forming a floating gate (40) in the trench along the sidewall and insulated therefrom; forming a first region (52) in said substrate along the bottom wall of the trench, with said first region being of a second conductivity type (N), different from said first conductivity type; forming a first gate electrode (54) in the trench, said first gate electrode insulated from said first region and capacitively coupled to said floating gate; forming a second region (70), of the second conductivity type (N) in said substrate, along the surface thereof, spaced apart from the trench; and forming a second gate electrode (68) spaced apart from the surface between said second region and said trench.

In re claim 18, an insulation material (56) between the second gate electrode and said floating gate with a thickness that permits Fowler-Nordheim tunneling of electrons from said second floating gate to said second gate electrode.

In re claim 19, an insulation material (36) between said floating gate and said bottom wall of said trench permitting the Fowler-Nordheim tunneling of electrons from said floating gate to said second region.

In re claim 20, the step of forming said floating gate includes forming said floating gate above the substrate surface. (Fig. 2q)

***Response to Arguments***

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on T-F 8:30-6:00 off Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

A handwritten signature in black ink, appearing to read "K. R. Rose".